Class Test 1

EEE 303: Digital Electronics

Total Marks: 20 Time: 15 minutes

Student Number: Date:

1. A circuit with two outputs has to implement the following functions

$f(x_1,x_2,x_3,x_4) = \sum m(4, 6, 7, 9, 11, 12, 14, 15) + D(1, 3)$
$g(x_1,x_2,x_3,x_4) = \sum m(1, 4, 9, 12) + D(3, 6, 14)$

Design the minimum cost circuit and compare its cost with combined costs of two circuits that implement *f* and *g* separately. Assume that the input variables are available both in uncomplemented and complemented forms. 20

Class Test 2

EEE 303: Digital Electronics

Total Marks: 20 Time: 20 minutes

Student Number: Date:

SET – A

1. A combinational circuit is defined by the following three functions:
   i. $F_1 = x'y' + xyz'$
   ii. $F_2 = x' + y$
   iii. $F_3 = xy + x'y'$

   Design the circuit with **only a decoder with an enabler pin** and **some external gates**.

2. Construct the truth table for a 4 to 2 input priority encoder with input priorities w_1, w_2, w_0, w_3 where w_1 **has the highest priority and** w_3 **has the lowest**. The output binaries are denoted as y_0 and y_1. Now, design the circuit for the encoder **using only 4 to 1 multiplexers**.

Class Test 2

EEE 303: Digital Electronics

Total Marks: 20 Time: 20 minutes

Student Number: Date:

SET – B

1. Construct the truth table for a 4 to 2 input priority encoder with input priorities w_1, w_3, w_0, w_2 where w_1 **has the highest priority and** w_3 **has the lowest**. The output binaries are denoted as y_0 and y_1. Now, design the circuit for the encoder **using only 4 to 1 multiplexers**.

2. A combinational circuit is defined by the following three functions:
   i. $F_1 = x' + y$
   ii. $F_2 = x'y' + xy$
   iii. $F_3 = xyz' + x'y'$

   Design the circuit with **only a decoder with an enabler pin** and **some external gates**.

Class Test 3

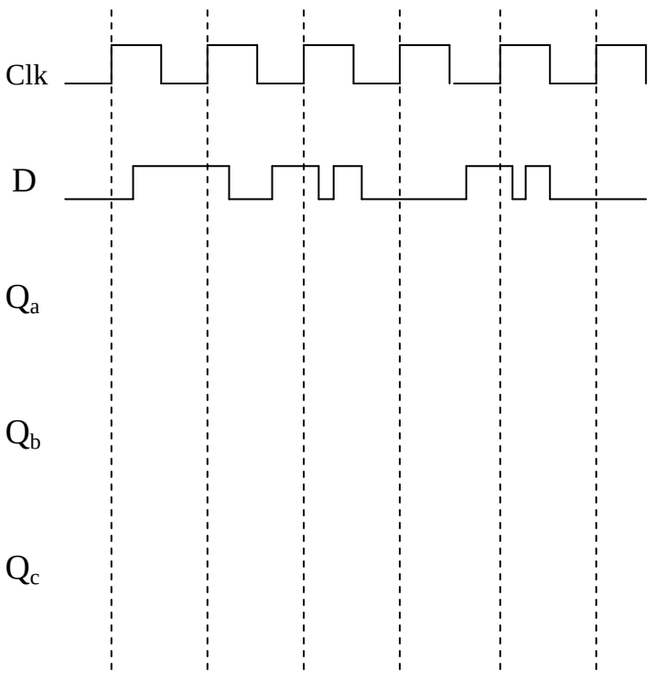
EEE 303: Digital Electronics

Total Marks: 20 Time: 20 minutes

Student Number: Date:

SET – A

1. Consider the following timing diagram. Assume that the D and Clock inputs are applied to the circuit in Fig. 1, draw waveform for the Q_a, Q_b and Q_c signals.



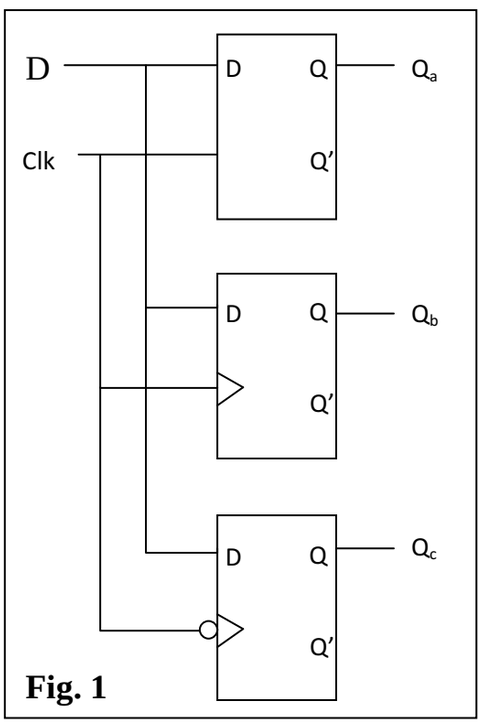


Fig. 1

2. Draw the circuit diagram of a three bit shift register using JK flip flops only.

Class Test 3

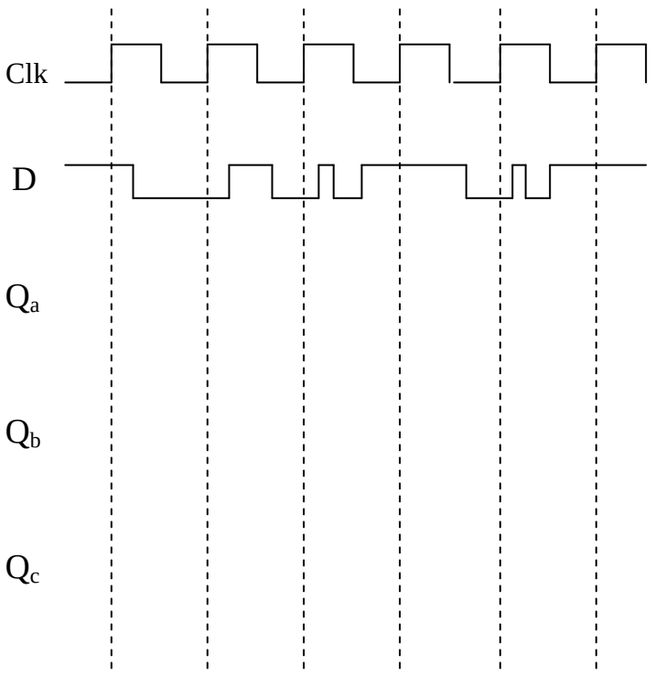
EEE 303: Digital Electronics

Total Marks: 20 Time: 20 minutes

Student Number: Date:

SET – B

1. Consider the following timing diagram. Assume that the D and Clock inputs are applied to the circuit in Fig. 1, draw waveform for the Q_a, Q_b and Q_c signals.



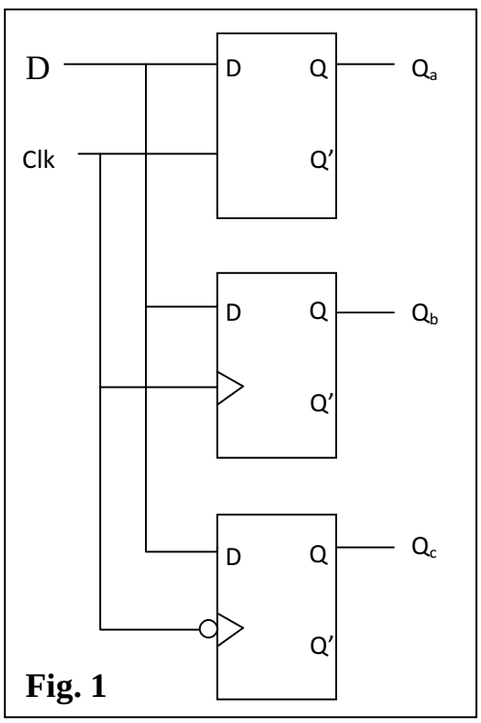


Fig. 1

2. Draw the circuit diagram of a three bit shift register using JK flip flops only.

Class Test 4

EEE 303: Digital Electronics

Total Marks: 20 Time: 20 minutes

Student Number: Date:

1. Using an ordinary 4-bit binary up counter and basic logic gates construct a 4-bit binary counter that counts in the sequence:
   1, 3, 6, 9, C, D, 1, 3, 6, 9, C, D…